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ROBERT A. SALTZBERG
MORRISON & FOERSTER LLP
425 MARKET STREET
SAN FRANCISCO, CA 94105

EXAMINER	
BUTLER, DENNIS	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 12/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/071,860	BOLT, THOMAS	
	Examiner	Art Unit	
	Dennis M. Butler	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-19,21-27 and 29-34* is/are rejected.

7)☒ Claim(s) *5,20 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This action is in response to the amendment filed on October 12, 2005. Claims 1-34 are pending.

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-4, 6-14, 16-19, 21-27 and 29-34 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification fails to describe selectively activating two of the devices at the same time as recited in independent claims 1, 9, 17 and 25. The examiner could find no description of selectively activating two of the devices at the same time in the specification other than what is recited in the claims. In the arguments applicant argues that Chong fails to disclose selectively activating two of the devices at the same time. The examiner pointed to column 6, lines 12-65 of Chong as disclosing the above limitation. Applicant has repeatedly denied that Chong's disclosure describes selectively activating two of the devices at the same time and argues that column 6, lines 12-65 of Chong teaches away from the claimed invention. However, the examiner can find no support for applicant's assertions in the specification. The specification seems to be silent as to the implementation of selectively activating two of the devices at the same time. Chong describes selecting a master/slave pair (two devices) using control register 26 and the

associated CS0 and CS1 select signals. Chong describes that devices 20A and 20B may be accessed (activated) when control register 26 contains the first value and signal routing logic 24 produces signals CS0 and CS1 as signals CS0A and CS1A respectively. Chong describes that devices 20C and 20D may be accessed (activated) when control register 26 contains the second value and signal routing logic 24 produces signals CS0 and CS1 as signals CS0B and CS1B respectively. Chong further describes that master/slave select bit 4 of an active devices command block register may be used to select between an active master device (20C) and an active slave device (20D). This clearly indicates that both the selected master and the selected slave devices are active. Otherwise there would be no need for select bit 4. In the prior rejections the examiner clearly pointed out that Chong's control register 26 and signal routing logic 24 allow only one pair of devices to be accessed at a time and clearly associated the accessible pair of devices with the claimed active devices. All unselected master/slave pairs of Chong are not capable of being accessed and cannot communicate over the ATA channel. Therefore, they are clearly not active. Furthermore, the ATA standard allows only two devices to be active or accessible on an ATA channel. Therefore, it is reasonable to interpret Chong's selected accessible devices as corresponding to the claimed simultaneously active devices. However, Applicant has repeatedly denied that Chong's disclosure describes selectively activating two of the devices at the same time and argues that column 6, lines 12-65 of Chong teaches away from the claimed invention. Applicant's specification fails to describe any details of selectively activating two of the devices at the same time. The specification is silent as to the

implementations of selectively activating two of the devices at the same time. Therefore, it is not possible for the examiner or the public to determine the difference between the prior art active/accessible devices and the claimed selectively activating two of the devices at the same time other than applicant's assertion that it is not what Chong discloses. Applicant should point out where there is support in the specification for the claimed selectively activating two of the devices at the same time limitation and applicant's arguments that this limitation is different from what is disclosed by Chong. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

4. The rejection under the second paragraph of 35 U.S.C. 112 is withdrawn in view of applicant's amendment to claim 33.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 17-19, 21, 23-27, 29 and 31-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Chong, Jr., U. S. Patent 6,697,867.

Per claims 17 and 25:

A) Chong, Jr. teaches the following claimed items:

1. an IDE interface system (ATA system) having three or more devices (ATA Devices 20A-D) connected to an IDE bus (ATA channel) with figure 1, at column 1, lines 13-25 and at column 5, lines 13-44;

2. a device controller for receiving device control signals to select at least one of the devices for data communication with the processor (CPU 12) with ATA Host Adapter 16 of figure 1 and at column 6, lines 1-11;

3. the device controller selectively activating at most two of the devices at the same time for data communication with the processor at column 6, lines 12-65.

Per claims 18-19, 21, 23-24, 26-27, 29 and 31-32:

Chong, Jr. describes receiving device control signals to select one or two of the devices for data communication with the processor (CPU 12) with ATA Host Adapter 16 of figure 1 and at column 6, lines 1-11, selecting one of the devices as a master device and the second device as a slave device and activating at most two of the devices at the same time for data communication with the processor at column 6, lines 12-65. Chong, Jr. describes deactivating (deasserting) non-selected devices at column 6, lines 44-53. Chong, Jr. describes a selection signal for each of the two devices with the CS signals that correspond to each of the devices at column 6, lines 12-65. Chong, Jr. describes

an interface controller connected to devices via the IDE bus for managing information flow between the processor and the devices with figure 1, at column 1, lines 13-25 and at column 5, lines 13-44. Chong, Jr. describes that at least one device is a disk drive at column 5, lines 59-67.

8. Claims 9-12 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chong, Jr., U. S. Patent 6,697,867 in view of Chu et al., U.S. Patent 6,725,385.

Per claims 9-11:

A) Chong, Jr. teaches the following claimed items:

1. an IDE system (ATA system) having three or more devices (ATA Devices 20A-D) connected to an IDE bus (ATA channel) with figure 1, at column 1, lines 13-25 and at column 5, lines 13-44;

2. identifying devices, selecting one of the devices as a master device and a second device as a slave device at column 6, lines 1-65,

3. activating at most two of the selected devices at the same time for data communication with the processor at column 6, lines 12-65.

B) The claim seems to differ from Chong, Jr. in that Chong, Jr. fails to explicitly describe deactivating all of the devices as claimed.

C) However, Chong, Jr. describes activating a device group using a group access signal and deactivating the remaining groups with corresponding group access signals at column 2, lines 25-34. Therefore, Chong, Jr. discloses the claimed invention except for explicitly reciting that all of the devices are

deactivated. Chu et al teach that it is known to deactivate all ATA devices connected to an ATA/IDE bus with figures 1 through 3, at column 1, lines 13-53, at column 2, lines 12-30 and at column 3, lines 45-67. In addition, Chu describes that deactivating all devices is a design choice based on a trade-off between energy consumption and response time of the devices at column 1, lines 13-19. It would have been obvious to one having ordinary skill in the art at the time the invention was made to deactivate all of the devices, as taught by Chu, in order to reduce the energy consumption of the devices connected to the IDE/ATA bus. One of ordinary skill in the art would have been motivated to combine Chong, Jr. and Chu because of Chu's suggestion that deactivating all devices connected to an ATA/IDE bus would reduce energy consumption of the system at column 1, lines 36-53 and at column 2, lines 54-65. It would have been obvious for one of ordinary skill in the art to combine Chong, Jr. and Chu because they are both directed to the problem of activating and deactivating ATA/IDE devices connected to an ATA bus. Furthermore, Chong, Jr. describes activating a device group based on a corresponding group access signal received from the host over the ATA interface at column 2, lines 15-18 and 25-34 and Chu describes providing monitoring logic that activates a device based on a predetermined communication signal over the ATA interface at column 2, lines 23-30. Therefore, the ATA power control features of Chu can be readily incorporated into the ATA interface of Chong, Jr.

Per claims 12 and 16:

Chong, Jr. describes connecting three or more devices to the IDE bus (ATA channel) at column 5, lines 36-44. Chong, Jr. describes that at least one device is a disk drive at column 5, lines 59-67.

Per claim 15:

Chu describes deactivating each device by powering them off and activating each selected device by powering them on with figure 2 and at column 6, lines 21-65.

9. Claims 33 and 34 rejected under 35 U.S.C. 103(a) as being unpatentable over Chong, Jr., U. S. Patent 6,697,867, in view of Lau et al., U. S. Patent 6,772,212.

Per claims 33 and 34:

Chong teaches the elements of claim 25 as described in the above rejection of claim 25. Chong describes selectively activating the devices for data communication as described in the above rejection of claim 25. The claims seem to differ from Chong in that Chong fails to explicitly teach a USB to IDE controller connected between the IDE bus and the processor as claimed. Lau teaches that USB to IDE interface controllers such as the OnSpec 90C36 were known and available on the market at the time of applicant's invention at column 5, lines 26-47. In addition, Lau teaches connecting a USB to IDE controller between the IDE bus (IDE connector 152 and associated lines to element 154) and the processor (computer) with figures 2 and 3 and at column 5, lines 16-47. It would have been obvious to one having ordinary skill in the art at the time the invention was made to connect a USB to IDE controller between the IDE bus and the processor, as

taught by Lau, in order to access IDT/ATA devices via a USB interface. One of ordinary skill in the art would have been motivated to combine Chong and Lau because of Lau's description that USB to IDE interface controllers such as the OnSpec 90C36 were well known in the IDE/ATA interface art, were available on the market and were used to interface IDE/ATA devices to USB ports at the time of applicant's invention. It would have been obvious for one of ordinary skill in the art to combine Chong and Lau because they are both directed to the problem of interfacing IDE/ATA devices to computer systems and Lau's teaching would allow Chong's ATA devices to be connected to CPU 12 using a USB port/interface.

10. Claims 5, 20 and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. Applicant's arguments filed on April 18, 2005 have been fully considered but they are not persuasive.

In the Remarks, applicant has argued in substance that:

A. Chong does not disclose a device controller that selectively activates two devices at the same time for data communication over the IDE bus.

B. Chong cannot activate any two devices at the same time and does not disclose utilizing a Cable Select signal as claimed in claims 17 and 25.

C. Chong does not disclose identifying one or two devices for data communication with the processor. There are only two ATA devices in either 21A

or 21B. Therefore, there is no need or disclosure in Chong for a step of identifying.

D. Chong does not disclose a device controller that selectively activates at most two or a maximum of two devices at the same time for data communication over the IDE bus.

E. There is no disclosure, suggestion or motivation in either Stryker or Chong of activating devices by powering them on and deactivating them by powering them off.

F. Chu does not mention or suggest connecting three or more IDE devices to an IDE bus. Chu is directed to a power controller that controls power consumption of a device. Chu has nothing to do with the present invention and is non-analogous art.

G. There is no suggestion or motivation in either Chong or Chu for combining them. The prior art itself must have an explicit teaching or suggestion to motivate one of ordinary skill to combine elements.

12. As to point A, the examiner disagrees with applicant's contentions that Chong does not disclose a device controller that selectively two devices at the same time for data communication over the IDE bus. Chong describes ATA Host Adapter selectively activating at most two devices using the CS0 and CS1 signals based on the contents of the control register at column 6, lines 12-43. Chong describes deactivating the remaining devices using the CS0 and CS1 signals based on the contents of the control register at column 6, lines 44-53. The activated devices are able to communicate over

the ATA channel as an ATA master/slave pair while the deactivated devices are not active for communication. Chong describes that devices 20A and 20B may be accessed (activated) when control register 26 contains the first value and signal routing logic 24 produces signals CS0 and CS1 as signals CS0A and CS1A respectively. Chong describes that devices 20C and 20D may be accessed (activated) when control register 26 contains the second value and signal routing logic 24 produces signals CS0 and CS1 as signals CS0B and CS1B respectively. Chong further describes that master/slave select bit 4 of an active devices command block register may be used to select between an active master device (20C) and an active slave device (20D). This clearly indicates that both the selected master and the selected slave devices are active. Otherwise there would be no need for select bit 4. In the prior rejections the examiner clearly pointed out that Chong's control register 26 and signal routing logic 24 allow only one pair of devices to be accessed at a time and clearly associated the accessible pair of devices with the claimed active devices. All unselected master/slave pairs of Chong are not capable of being accessed and cannot communicate over the ATA channel. Therefore, they are clearly not active. Furthermore, the ATA standard allows only two devices to be active or accessible on an ATA channel. Therefore, it is reasonable to interpret Chong's selected accessible devices as corresponding to the claimed simultaneously active devices. Furthermore, as described above in connection to the 112, first paragraph rejection, there is no support in applicant's specification for applicant's assertion that Chong's selected accessible devices are not active. The specification is silent as to simultaneously activating devices as recited in the rejected

claims. If there is support in the specification, applicant should point to the evidence that supports this assertion.

As to point B, claims 17 and 25 do not recite activating any two devices at the same time or utilizing a Cable Select signal. Therefore, it is irrelevant whether Chong discloses these features. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

As to point C, the examiner disagrees with applicant's contentions that Chong does not disclose identifying one or two devices for data communication with the processor, that there are only two ATA devices in either 21A or 21B and that there is no need or disclosure in Chong for a step of identifying. As described in detail in the above art rejection, Chong describes interfacing more than two ATA devices to the same ATA channel by coupling multiple groups of devices to the channel at column 1, line 61 – column 2, line 18. Chong describes that the groups of devices may be master/slave pairs or a single device at column 3, lines 1-10. Chong describes providing routing logic in the form of a 1-to-p demultiplexer coupled to a control register to route an access signal from the host system to the selected group dependent on the value stored in the control register at column 2, lines 53-58. Chong describes that CPU 12 accesses the ATA devices via the ATA host adapter by executing instructions of ATA driver software 22 with figure 3 and at column 5, lines 61-67. Chong describes that one or two devices are identified for data communication with the group access signal and with the value stored in control register 26 with figure 4 and at column 9, lines 36-49. The examiner

disagrees with applicant's statement that there are only two ATA devices in either 21A or 21B and therefore, there is no need or disclosure in Chong for a step of identifying. As previously described in both the art rejection and the above arguments, Chong describes interfacing more than two ATA devices to the same ATA channel by coupling multiple groups of devices to the channel at column 1, line 61 – column 2, line 18, with figure 1, at column 2, lines 53-58 and at column 3, lines 1-10. Chong's entire disclosure is directed to coupling more than two devices to a single ATA interface channel. Applicant's statements are a refusal to acknowledge the teachings of the prior art rather than a failure of Chong to disclose coupling more than two devices to a single ATA channel and identifying and selecting one or two of the devices for data communication. In addition, it is unclear why applicant continues to make this assertion. The assertion appears to be unfounded and without merit in view of Chong's detailed description of selecting devices 20A through 20D. Applicant is requested to describe why he believes Chong has no need for identifying devices rather than just continue to make this unfounded assertion. Applicant is requested to address Chong's control register 26 and the value written to this register, the generation of the correct CS signal (CS0A, CS0B, CS1A and CS1B) for accessing a desired ATA device and the generation of the master/slave select bit 4 of each drive/head command block register in the description of why Chong has no need for identifying devices.

As to point D, the examiner disagrees with applicant's contentions that Chong does not disclose a device controller that selectively activates at most two or a maximum of two devices at the same time for data communication over the IDE bus.

Chong describes ATA Host Adapter selectively activating at most two devices using the CS0 and CS1 signals based on the contents of the control register at column 6, lines 12-43. Chong describes deactivating the remaining devices using the CS0 and CS1 signals based on the contents of the control register at column 6, lines 44-53. The activated devices are able to communicate over the ATA channel as an ATA master/slave pair while the deactivated devices are not active for communication.

As to point E, the examiner disagrees with applicant's contentions that there is no suggestion or motivation in either Stryker or Chong of activating devices by powering them on and deactivating them by powering them off. There is clear suggestion and motivation for activating devices by powering them on and deactivating them by powering them off in both Stryker and Chong. Stryker describes four methods of activating and deactivating ATA devices including using the CSEL line, intercepting the DRV/HD command and using Q-switches. Chong, Jr. describes activating and deactivating ATA devices using group access signals, a control register, routing logic and chip select signals. Therefore, both references describe how to couple more than two devices to a single ATA channel by activating one or two devices at the same time for communication over the channel. Both references teach that the solution to coupling more than two devices to a single ATA channel is to activate one or two devices at the same time while deactivating the remaining devices. Both references describe a plurality of ways to activate and deactivate the devices. Therefore, both references teach that there are a plurality of ways to implement the disclosed solution of activating and deactivating devices for communication. It would have been obvious to one having

ordinary skill in the art at the time the invention was made to activate the selected devices by powering the devices on and deactivate the remaining devices by powering them off because it is well known and inherent that ATA devices cannot be active when they are powered off and using the device power inputs for activating and deactivating the devices would reduce the power consumption of the ATA/IDE system. There is clear suggestion and motivation for activating devices by powering them on and deactivating them by powering them off in both Stryker and Chong.

As to point F, the examiner disagrees with applicant's contentions that Chu does not mention or suggest connecting three or more IDE devices to an IDE bus. Chu is directed to a power controller that controls power consumption of a device. Chu has nothing to do with the present invention and is non-analogous art. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). As to Chu being non-analogous art, the examiner disagrees with applicant's contention, Chu is clearly analogous. Applicant's claims recite deactivating all IDE devices connected to an IDE bus. Applicant's specification describes that logic device 16 includes power control circuitry used to control the power to each IDE device as well as activate and deactivate devices at paragraphs 19, 28 and 29. Chu describes the details of implementing power control in an IDE/ATA device including monitoring signals, deactivating all devices, activating devices and described the trade-off between energy consumption and

response time. Chu teaches the power control aspects of the claimed invention. Therefore, Chu is analogous art. Chu describes controlling the power to IDE/ATA devices by placing them in a reduced power state so that they are not active or able to communicate data over the ATA bus and activating (powering) a device upon detecting that a host is communicating with the device. The claimed invention is clearly obvious in view of the combination of the references.

As to point G, the examiner disagrees with applicant's contentions that there is no suggestion or motivation in either Chong or Chu for combining them. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case Chu's suggestion that deactivating all devices connected to an ATA/IDE bus would reduce energy consumption of the system as well as deactivate devices not selected for communication. The normal desire of scientists or artisans to improve upon what is already generally known provides the motivation to determine where in a disclosed set of percentage ranges is the optimum combination of percentages. In re Peterson (1/8/03). One of ordinary skill in the art would have been motivated to combine Chong, Jr. and Chu because of Chu's suggestion that deactivating all devices connected to an

ATA/IDE bus would reduce energy consumption of the system at column 1, lines 36-53 and at column 2, lines 54-65. It would have been obvious for one of ordinary skill in the art to combine Chong, Jr. and Chu because they are both directed to the problem of activating and deactivating ATA/IDE devices connected to an ATA bus. Furthermore, Chong, Jr. describes activating a device group based on a corresponding group access signal received from the host over the ATA interface at column 2, lines 15-18 and 25-34 and Chu describes providing monitoring logic that activates a device based on a predetermined communication signal over the ATA interface at column 2, lines 23-30. Therefore, the ATA power control features of Chu can be readily incorporated into the ATA interface of Chong, Jr.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis M. Butler whose telephone number is 571-272-3663. The fax number for this unit is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dennis M. Butler
Primary Examiner
Art Unit 2115